REMARKS

I. Status of Claims

The Examiner stated in his advisory action dated 3/31/2006 that "the amended claims and added new claim*[sic]* overcome the rejection under §103 per combined references to Rahut and Chen." This implies that the amendments were entered and only one new claim added. However, the examiner has also indicated at least twice in the advisory action that the proposed amendments and new claims were not entered. Consequently, it is again unclear which claims are pending.

Therefore, Applicants again assume throughout the present response that the Examiner examined the claims submitted on December 2, 2005 and Applicant submits amendments to the claims accordingly herein. Specifically, claims 1-4 are pending. Claims 1 and 3 are amended herein. Claims 5 and 6 have been added to more clearly point out and distinctly claim what Applicants believe their invention to be. No new matter has been added. Applicants respectfully request that the amendments be entered.

To avoid future confusion, Applicants respectfully request that the Examiner expressly and unambiguously state in his next office action which set of claims were examined in the final office action, advisory action, and this action.

II. Claim Objections

The Examiner has objected to claims 1 and 3 for certain antecedent informalities. These claims have been amended to correct the informalities and Applicants believe the claims are now in proper form. Applicants respectfully request that the Examiner withdraw this objection.

III. Claim Rejection Under 35 USC §103

The Examiner has rejected claims 1-4 as being obvious over Rahut in view of Chen. A claim is *prima facie* obvious only if the prior art reference (or references when combined) teach or suggest all the claim limitations. MPEP §2143. It is

improper to combine references when one teaches away from the combination. MPEP §2146 and *In re Grasselli, 218 UPQ 769, 779 (Fed. Cir. 1983).*

A. Rahut Does Not Disclose Disregard of Fan-out

As to claims 1 and 3, the Examiner states that Figures 1-3 and column 4, lines 23-37 of Rahut teach "an FPGA behaving in a way that timing is... affected negligibly by fanout..." See paragraphs 5 and 7 of the present office action. However, Rahut does not teach that limitation in the cited locations or elsewhere. Indeed, the sections in Rahut cited by the Examiner affirmatively discuss determining which routes to analyze for delay reduction because, by limiting the number of routes analyzed, the design is less constrained. See Rahut column 4, lines 27-37. It is inherent that, if the designer has to choose which routes to analyze for delay, that all routes have some effect on the timing. Rahut goes on to say that "By routing one or more critical connections of selected logic level, downstream connections ... are made less critical." Again, Rahut teaches that downstream connections are not negligible, but are critical (maybe less so than others). Thus, Rahut does not disclose the claimed limitation and, moreover, teaches away from a method that uses a FPGA in which timing is affected negligibly by fanout.

Therefore, Applicants believe Rahut does not disclose this limitation and therefore a prima facie case of obviousness has not been established. Moreover, even if Rahut discloses the limitation, Rahut teaches away from the limitation and therefore Rahut and Chen cannot be combined. Applicants respectfully request that the obviousness rejections be withdrawn.

B. Neither Rahut Nor Chen Discloses Operatively Substituting of The Elements Utilized In The First Placement

As to claims 1 and 3, the Examiner admits that Rahut does not teach change being a change in selecting logic elements and placement of those elements. ..." See paragraphs 5 and 7 of the present office action. The Examiner implies that Chen discloses a duplicate module 408 [*sic* 405] in Fig. 4 that selects

logic elements on the critical path and replicates them. Id. However, Chen does not disclose such a limitation.

Chen's duplicate module 405 stores with each component a list of the one or more clusters to which the component belongs. Chen, column 15, lines 59-61. This is simply a reference list, not a duplication of functioning logic elements. Chen does disclose that when two clusters are assigned to different clocked FPGAs, the components common to the two clusters are duplicated in both FPGAs. Chen, column 16, lines 41-43. However, ***both*** of those components are used in the emulation, one on each FPGA, to prevent having to route a common signal outside one FPGA to another. That is, both sets of logic elements run at the same time. Chen does not teach or suggest the substitution of a set of logic elements.

As amended, claim 1 requires duplicating logic gates "operatively ***substituting*** [for] the first placement and being a selection of logic elements to implement the critical path." That is, ***only one*** of the sets of logic elements are used in Applicants' invention. The first set remains dormant during use and only the second set is used because the second placement is faster than the first placement.

Therefore, Applicants believe that Chen does not teach or suggest the duplication and substitution of a set of logic elements. Therefore, because the cited references do not teach or suggest one of Applicants' claimed limitations, no *prima facie* case has been established. Applicants respectfully request that this rejection be withdrawn.

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CONCLUSION

Applicants respectfully submit that all objections and rejections have been traversed, and that the application is in form for issuance.

Respectfully submitted,

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Dated

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